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REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed on August 9, 2006. The Office Action has rejected claims 13-17 and 25-36 under 35 U.S.C. § 102(b) as being anticipated by Rajeevakumar (USP 5,426,324; hereinafter Rajeevakumar). The Office Action has further rejected claims 18-24 as being anticipated by Jeon (USP 5,455,192, hereinafter Jeon).

Claims 13 and 25 have been amended and claims 35 has been cancelled to more accurately describe the present invention. Claims 18-24 remain cancelled from the amendments submitted on December 30, 2005. Claims 37-43 have been newly added. Upon entry of the amendments, 13-17, 25-34, and 36-43 remain pending. It is believed that no new matter is added by way of these amendments made to the claims or otherwise to the application.

After carefully considering the remarks set forth in this Office Action and the cited references, Applicants respectfully submitted that the presently pending claims are already in condition for allowance. Reconsideration and withdrawal of the Examiner's rejection are requested.

Claim Rejections-35 USC §102

The Office Action rejected claims 13-17, 25-36 under 35 U.S.C. 102(b) as being anticipated by Rajeevakumar (US Patent 5,426,324).

Applicant appreciates the Examiner's proposal, dated July 21, 2006, of amending claims 13 and 25 by inserting the limitation "*wherein the capacitor dielectric layer continuously extends from inside the trench to an upper surface of the substrate*" to render the claims allowable. In response thereto, Applicant has amended claims 13 and 25 by inserting the limitation suggested by the Examiner.

In essence, Rajeevakumar teaches the capacitor dielectric layer being formed to about the mid-section of the trench, while the top section of the trench is formed with the collars 31. Accordingly, Rajeevakumar has at least fails to teach or suggest each and every element in claims 13 and 25. Withdrawal of the rejection is thus courteously requested.

The Office Action rejected claims 18-24 under 35 U.S.C. 102(b) as being anticipated by Jeon (US Patent 5,455,192)

Claims 18-24 had been previously cancelled to render the 35 U.S.C. §102(b) rejection by Jeon moot. However, the applicant has added new claims 37-43, in which claim 37 is written in independent form describing a dynamic random access memory cell comprising a substrate having a trench; a conducting layer filling said trench and extending to said substrate around said trench, wherein a top surface of the conducting layer is aligned with an upper surface of the substrate; a capacitor dielectric layer continuously extending from inside the trench to the upper

surface of the substrate between a surface of said trench and said conducting layer, and between said conducting layer and said substrate, said conducting layer being an upper electrode, and said substrate around said capacitor dielectric layer being a bottom electrode; a gate electrode on said substrate beside said conducting layer; a plurality of drain/source regions in said substrate beside two sides of said gate electrode; and a gate dielectric layer between said gate electrode and said substrate. Claims 38-43 are depended on the allowable claim 37.

Applicant respectfully submits the newly added claims are differentiable from Jeon for at least the following reasons.

Jeon teaches the polysilicon layer 64 filling the trench and extending above the top surface of the substrate to form the trench capacitor and the stack capacitor (the first polycrystalline silicon 56 of the stack capacitor is the part of the polysilicon layer 64 above the top surface of the substrate). Accordingly, Jeon at least fails to teach a top surface of the conducting layer that fills the trench is aligned with an upper surface of the substrate. Moreover, the word line 50 of Jeon is formed under the polysilicon layer 64, whereas the gate electrode 208a of the invention is formed above the conductive layer 204. Further, the invention teaches that the capacitor dielectric layer is configured between the conducting layer and the substrate. Jeon, however, teaches that the dielectric layer 62 is configured between the first polysilicon layer 56 and the second polysilicon layer 64.

For at least these reasons, Applicant respectfully asserts that Jeon fails to teach or suggest the present invention or to render claim 37 anticipated. Since claims 38-43 are dependent claims, which further define the invention recited in claim 37, Applicants

respectfully assert that these claims also are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively requested.

Conclusions

In light of the foregoing amendments and for at least the reasons set forth hereinbefore, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 13-17, 25-34, and 36-43 are in condition for allowance. Favorable consideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned.

Respectfully submitted,
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